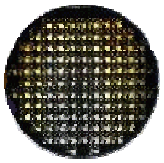

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# Known-Good-Die Assurance for MCMs in Space Application

## Introduction

The trends in VLSI and ULSI packages are toward more and more terminal count, higher speed devices, higher thermal dissipation, and higher packaging densities. Multichip Modules (MCMs), apart from traditional hybrids, are providing high density interconnections, high design integration, and flexibility. MCMs are defined one way as complex hybrid microcircuits containing several interconnected active elements; the level of integration is very high and few or no passive components are used. Active elements in an MCM may include simple hybrid microcircuits or complex VLSI/ULSI microcircuits. This specialized approach to packaging and design integration is currently one of the fastest growing segments of all packaging technologies. This approach has invaluable benefits to systems used in space applications for both ground support or actual flight hardware. The design of MCMs is complex and must deal with the issues of materials, system architecture, electrical and mechanical performance, economics, and reliability. In this discussion, reliability issues and concerns are reviewed especially as they apply to Known-Good-Die and their qualification.

## Known-Good-Die Reliability

Multichip packaging is defined as: 1) two or more bare chips directly attached to a multichip substrate or, 2) two or more prepackaged chips attached on a multichip substrate. In either case the chips (die) must be free of defects as received and remain defect free and functional after assembly. Hence, the term defect free die is also known as "Known-Good-Die". The term, "die" is also used here interchangeably with Integrated Circuits (ICs). The ICs used in MCMs are becoming more and more dense with transistors by using advanced scalar technologies, and often mixing different technologies on the same IC. These advancements now compound the task of assuring the ICs are good and reliable in an MCM as compared to ICs in single packaging. The primary reason is that single package microcircuits can be tested

and qualified to a higher level of confidence in functionality, performance, and reliability than bare ICs (die). Some manufacturers claim that single packaged die can be assured with 0.99999 probability that the die are electrically good and very reliable, while die alone can only be assured from 0.50 to 0.99 probability that they are electrically good and marginally reliable. This reliability will vary according to manufacturer and maturity of technology and product. Increasing the number of die in an MCM reduces the MCM yield and reliability even further. A simple expression used to illustrate this is $Yin = 100(Pc)^n$, where Yin is the probable percent yield for assemble modules, n is the number of ICs in the module, and Pc is the probability that an IC is known-good.

Known-Good-Die Test Issues

The testing of bare die by semiconductor manufacturers typically falls short of what is required for use in MCMs. The normal testing of packaged die includes wafer parametric testing after fabrication, wafer sort testing, and final package testing after assembly. In addition, pre and post bum-in testing may be performed before shipping the product. Cumulative testing and the effectiveness of each of these tests increases the probability (Pc) that the passing packaged die is good and reliable. For MCMs using bare die, only wafer sort testing is available in most manufacturing flows. Most testing performed at the wafer level has not been adequate to ensure that the die is defect free and reliable to 0.99999 probability. Two reasons for this inadequacy are limitations to testing die at high performance speeds and testing at high and low temperature extremes. In addition, there are considerable differences in dc and ac test coverage for die versus packaged die. These differences are governed by differences in the test software programs, and performance characteristics due to test fixtures and the packaging. It has been demonstrated that die tested good in one package type may not function properly in another package type. If this problem is caused by parasitic capacitance within the package, the manufacturer can make some test adjustments during the die testing for compensation. For MCMs this approach may be costly once the die are attached to the substrate.

Burning-in packaged die to accelerate the processe failure mechanisms that cause units to fall, is part of most high reliability flows used in flight applications. Although some manufacturers claim that modem technologies are better, microcircuits can still fail in the field because of latent defects undetected prior to shipping to the customer. In fact, modern technologies should be fully qualified to be defect free before one accepts any claims by the manufacturer. Burn-in has been very effective in eliminating intrinsic defects within the die and

has shown devices to have abnormal electrical behaviors as compared to the rest of the population from the same lot. Again, removing these devices from use improves the Pc toward 0.99999. Because of the nature of different intrinsic defects, different bum-in methods are used to accelerate them. For MCMS, these proven methods are often not applicable nor feasible. Some believe that as manufacturers improve their processes the need for IC bum-in is no longer necessary. However, until new processes and technologies reach a high level of demonstrated maturity, there is risk in not performing IC bum-in such as MCM rework to replace defective ICs or long term MCM failure.

Environmental stress screening (ESS) is another means of revealing the presence of mechanical, chemical, and other defects, which might lead to die or package failure during the service life of the part. A circuit may initially operate properly, yet, have a material weakness. The problem addressed by ESS is the detection of those defects which mechanically or chemically weaken the part such that failure occurs subsequent to testing and after field deployment. In some instances, hybrid circuits have had electrical failures caused by interaction of the die with package plating. For MCMS, the issue is how to perform ESS to detect such interaction caused by various contaminates. To minimize these contamination factors, various passivation and die protection schemes are used. These passivation films provide for diffusion barriers, moisture barriers, and alpha particle barriers. The Known-Good-Die process needs assurance that these passivation films are reliable for the MCM and its application.

## Known-Good-Die Assurance

The above issues and concerns must be addressed to assure that the die used in MCM assembly are defect free and reliable. Some actions to be taken should include: 1) better process controls during the manufacturing of bare die through continuous process improvements, 2) using advanced test structures on the wafer to qualify the die wafer by wafer, 3) design for reliability and test on the die to enable high speed testing over temperature, 4) use of non-contact testing built-in self-test features , 7) >99.99% fault coverage simulations, 8) static functional testing, 9) dynamic functional testing, 10) radiation tolerance, 11) statistical sampling of die lots using packaged tests and ESS, 12) IDDQ testing with BI, and 13) BAMBI screenings. There is a real need to define MCM/KGD flight requirements to assure minimum rework, cost, and reliability. Subsequently it will be necessary to carefully optimize between the user's requirements and the manufacturer's KGD qualification when selecting from among different manufacturer technologies/flows.